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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,385	12/31/2003	Lance Weston	H0006069-555	8983
	7590 11/12/200 INTERNATIONAL, 1	EXAMINER		
LAW DEPARTMENT			DINH, TUAN T	
101 COLUMBIA ROAD MORRISTOWN, NJ 07692			ART UNIT	PAPER NUMBER
			2841	
			MAIL DATE	DELIVERY MODE
			11/12/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)			
	10/750,385	WESTON ET AL.			
Office Action Summary	Examiner	Art Unit			
	Tuan T. Dinh	2841			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).					
Status					
1)⊠ Responsive to communication(s) filed on <u>29 Ju</u>	ılv 2006.				
	action is non-final.				
· <u> </u>	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is				
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
·	pane Quayio, 1000 0.21 1.1, 10	3 3.3.2.3.			
Disposition of Claims					
 4) Claim(s) 1-12 and 27-89 is/are pending in the application. 4a) Of the above claim(s) 1-12 and 27-61 is/are withdrawn from consideration. 5) Claim(s) 71-75 and 85-89 is/are allowed. 6) Claim(s) 62-70,76-84 is/are rejected. 7) Claim(s) is/are objected to. Claim(s) are subject to restriction and/or election requirement. 					
Application Papers					
 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. 					
Priority under 35 U.S.C. § 119					
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 					
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	te			

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DETAILED ACTION

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 62-70, 76-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laschinski (U.S. Patent 6,467,163) in view of Tanabe et al. (U.S. Patent 4,883,920).

As to claims 62, 76, Laschinski discloses a universal component mounting structure for surface mountable electronic devices as shown in figures 1-2 comprising:

a printed circuit board (2, column 3, lines 60-61) having a SMT component (16) mounted on, the component (30; 40) having first and second terminals (column 5, lines 23-24), and each terminals having a first edge;

a conductive trace (10) formed on the PCB (2) having first and second opposed edges extending intermediate said first and second terminals (see figure 2), the edges of the trace (10) being defined a plane, see figure 2 and intersecting the first edge of the first and second terminals, the edge of the trace (10) disposed in parallel spaced relative to the edge of the first and second terminals respectively.

Laschinski does not specifically disclose the SMT component (16) having end caps. Tanabe et al. teaches a SMT component (2) having end caps (4) mounted on a

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substrate (1). It would have been obvious to one having an ordinary skill in the art at the time the invention was made to have the SMT component having end caps as taught by Tanabe et al. employed the SMT component of Laschinski in order to easy install components mounted on the PCB.

As to claims 66, 80, Laschinski discloses a universal component mounting structure for surface mountable electronic devices as shown in figures 1-2 comprising:

a printed circuit board (2, column 3, lines 60-61) having a first SMT component (16) mounted on, the component (30; 40) having first and second terminals (column 5, lines 23-24), and each terminals having a first edge; and a second SMT component (14) having end caps (see figure 2), and

a conductive trace (10) formed on the PCB (2) having first and second opposed edges extending intermediate said first and second terminals (see figure 2), the edges of the trace (10) being defined a plane, see figure 2 and intersecting the first edge of the first and second terminals, the edge of the trace (10) disposed in parallel spaced relative to the edge of the first and second terminals respectively.

Laschinski does not specifically disclose the SMT component (16) having end caps. Tanabe et al. teaches a SMT component (2) having end caps (4) mounted on a substrate (1). It would have been obvious to one having an ordinary skill in the art at the time the invention was made to have the SMT component having end caps as taught by Tanabe et al. employed the SMT component of Laschinski in order to easy install components mounted on the PCB.

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Regarding claims 63-65, 67-70, 77-79, and 81-84, Laschinski as modified by Tanabe et al. do not discloses either the second edge of the trace and the first edge of the second cap substantially equal to X (X = 0.01 in).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have X dimension of 0.01 in equal to either the second edge of the trace and the first edge of the second cap in order to minimize size of the PCB, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level Of ordinary skill in the art. In re Rose 105 USPQ 237 (CCPA 1955).

Allowable Subject Matter

3. Claims 71-75, and 85-89 are allowed.

The following is an examiner's statement of reasons for allowance: the prior arts do not teach or suggest in combination of the system having a second conductive trace on a printed circuit board having first and second opposed edges extending intermediate first and second end caps of a third surface mount component, said first and second opposed edges of said second conductive trace being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap of said third surface mount component and intersecting said first edge of said second end cap of said third surface mount component, said first edge of said second trace being disposed in parallel spaced relation to said first edge of said first end cap of said third surface mount component and said second edge of said second trace being disposed in parallel

spaced relation to said first edge of said second end cap of said third surface mount component (claims 71 and 85).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

4. Applicant's arguments filed 07/29/09 have been fully considered but they are not persuasive.

Applicant argues:

A. Neither reference relied on relates to the problem of transient protection or dissipating transients or even mentions the word "transients" or any synonym thereof. Neither reference relied on relates to any solution for dissipating transients.

Response to (A), Examiner disagrees because the term "for transient protection or dissipating transients" is preamble language and "for plus function" for the circuit protection system. Further, the preamble language or "for plus function" must be read on the context of the entire claim or in a body of the claim. So the term "for transient protection or dissipating transients" does not support in the body of the claimed invention.

B. The reference does disclose lands (10) for only attachment of device terminals and does not teach the land that is intermediate the edges of the terminals of the component.

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Examiner disagrees because the examiner is confused what does applicant means.? The land pattern (10) is formed on a PCB and <u>intermediate between</u> the terminals of the component, see figure 2.

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C) Laschinski in addition to not describing surface mount components that include end caps, clearly does not describe or even mention the dimensions X and t dimensions as defined in the present specification and claims of the present application much less identify the importance of these dimensions in any embodiment in the reference.

Examiner disagrees because as modified by Tanabe, Tanabe et al. teaches a SMT component (2) having end caps (4) mounted on a substrate (1). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to have the SMT component having end caps as taught by Tanabe et al. employed the SMT component of Laschinski in order to easy install components mounted on the PCB, and it would have been obvious to one having ordinary skill in the art at the time the invention was made to have X dimension of 0.01 in equal to either the second edge of the trace and the first edge of the second cap in order to minimize size of the PCB, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level Of ordinary skill in the art. In re Rose 105 USPQ 237 (CCPA 1955).

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lee Jinhee can be reached on 571-272-1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T Dinh/ Primary Examiner, Art Unit 2841.